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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,022	08/02/2001	Guy Harlan Humphrey	10010504-1	7798

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AGILENT TECHNOLOGIES, INC.
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EXAMINER

NGUYEN, MINH T

ART UNIT PAPER NUMBER

2816

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/921,022

Applicant(s)

HUMPHREY, GUY HARLAN

Examiner

Minh Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 12-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 12-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 September 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/13/03 has been entered.

Claim Objections

2. Claims 6 and 17 are objected to because of the following informalities:

In claim 6, line 1, "3" should be changed to --5-- because claim 3 does not have one or more additional switchably conductive devices.

In claim 17, the same problem exists as noted in claim 6, and further, the limitation one or more additional switchably conductive devices should be added to avoid double patenting problem, i.e., see claim 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 7, 12, 14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,036,222, issued to Davis (note that all the references used in this Office Action are cited in the previous Office Actions, therefore, copy of references will not be sent).

As per claim 3, Davis discloses an apparatus (Fig. 3) for reducing the slew rate of transition edges of a digital signal on a node (VOUT) of an integrated circuit, comprising:

a first switchably conductive device N1 (N1 is seen as a switchably conductive device because N1 can be controlled ON/OFF by a signal applying to the gate of N1) characterized by a first threshold voltage (the voltage which starts to turn ON FET N1) having a control input (the gate) connected to receive a driving signal (the signal at the gate of N1), since it is known that a threshold voltage of a NFET is the voltage in which above this voltage the NFET is ON and below this voltage the NFET is OFF, the limitation recited on lines 7-10 is met; and

a second switchably conductive device (the combination of P4 and N2-N3, i.e., consider a “blackbox” which covers P4 and N2-N3 having an input terminal connected to the gate of N1, another terminal connected to (VOUT) and a further terminal connected to GND) characterized by a second threshold voltage which is greater than the first threshold voltage (see column 10, lines 16-36 for the description, i.e., when a driving signal is applied to the gate of N1 and also the input terminal of the “blackbox”, N1 is ON first when the driving signal reaches the first threshold voltage, and allowing current flows from VOUT to GND through N1, and when the driving signal reaches the second threshold voltage, the second switchably conductive device, the “blackbox”, is ON by allowing current flows from VOUT to GND through the “black box”, from

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the terminal VOUT to the further terminal of the “blackbox”, Davis further explicitly discloses such operation as “bifurcated turn on”, column 10, line 35, to reduce the slew rate of the output driver).

As per claim 1, this claim is merely a method to operate an apparatus having the structure discussed in claim 3 above, since Davis teaches the circuit, he inherently teaches the method.

As per claim 7, this claim is rejected for the same reasons noted in claim 1.

As per claim 14, Davis discloses an apparatus (Fig. 3) for reducing the slew rate of transition edges of a digital signal on a node (VOUT) of an integrated circuit, comprising:

a first switchably conductive device P1 (P1 is seen as a switchably conductive device because P1 can be controlled ON/OFF by a signal apply to the gate of P1) characterized by a first threshold voltage (the voltage which starts to turn ON transistor P1) having a control input (the gate) connected to receive a driving signal (the signal at the gate of P1), since it is known that a threshold voltage of a PFET is the voltage in which above this voltage the PFET is OFF and below this voltage the PFET is ON, the limitation recited on lines 7-10 is met; and

a second switchably conductive device (the combination of N4 and P2-P3, i.e., consider a “blackbox” which covers N4 and P2-P3 having an input terminal connected to the gate of P1, another terminal connected to (VOUT) and a further terminal connected to VCC) characterized by a second threshold voltage which is less than the first threshold voltage (see column 10, lines 60-68 to column 11, line 1-15).

As per claim 12, this claim is merely a method to operate an apparatus having the structure discussed in claim 14 above, since Davis teaches the circuit, he inherently teaches the method.

As per claim 18, this claim is rejected for the same reasons noted in claim 12.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 5 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,036,222, issued to Davis in view of US Patent No. 5,877,647, issued to Vajapey et al.

As per claim 5, Davis teaches an apparatus (Fig. 3) for reducing the slew rate of a digital signal which comprises first and second switchably conductive devices having first and second threshold voltages as discussed in claim 3 above but he does not explicitly teach an apparatus which comprises one or more additional switchably conductive devices wherein each has different threshold voltage as called for in the claim.

Vajapey discloses an apparatus (Fig. 6) for controlling the slew rate of an output signal using switchably conductive devices P1 and P2, and in column 7, lines 1-5, he explicitly suggests another embodiment which has one or more additional switchably conductive devices to further control the slew rate of the digital signal at the node.

It would have been obvious to one skilled in the art at the time of the invention was made to add one or more switchably conductive devices to the Davis's circuit wherein each has different threshold voltage.

The motivation/suggestion for doing so would have been obvious for the reason discussed herein above, i.e., more control of the slew rate of the digital signal at the node VOUT of the Davis's circuit.

Therefore, it would have been obvious to add one or more additional switchably conductive devices to the Davis's circuit shown in Fig. 3 to obtain the invention specified in the claim.

As to the functional limitation recited on lines 7-12 of the claim, the combination discussed herein above clearly functioned as recited.

As per claim 2, rejected for the same reasons and motivations noted in claim 5.

As per claims 13 and 16, rejected for the same reasons and motivations noted in claims 2 and 5, respectively.

5. Claims 4, 15, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,036,222, issued to Davis in view of US Patent No. 4,386,286, issued to Kuo.

As per claim 4, Davis discloses the first switchably conductive device N1 comprises a single FET N1, and the second switchably conductive device comprises FETs N2-N3, P4, but he does not disclose the second switchably conductive device comprises a single FET as called for in the claim.

Kuo discloses (in Fig. 1) first and second FETs 24 and 25 connected in parallel wherein the gates receive the CS signal, FETs 24 and 25 having different threshold voltages (column 2, lines 41-48 and column 3, lines 23-28) for turning on FETs 24 and 25 at different voltages.

It is notoriously well-known in the semiconductor art that fabricating FETs having the same threshold voltages in a semiconductor chip is easier and cheaper than fabricating FETs having different threshold voltages in a semiconductor chip, however, the later results in less number of FETs required, and therefore, the integrated circuit is more compact.

It would have been obvious to one skilled in the art at the time of the invention was made to replace the Davis second switchably conductive device comprises FETs N2-N3, P4 by a single FET having different threshold voltage than the first switchably conductive device.

The motivation and suggestion for doing so would have been to produce a more compact integrated circuit for applications which require less space occupied.

As per claim 15, this claim is rejected for the same reasons and motivation as discussed in claim 4.

As per claim 19, this claim is rejected for the same reasons and motivations noted in claim 4.

As per claims 20-21, these claims merely recite methods to operate the apparatus having the structure discussed in claim 4 herein above. Since the structure is disclosed as discussed, the methods to operate such a circuit would be obvious to a person skilled in the art.

6. ^{my} Claims 6, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,036,222, issued to Davis in view of US Patent No. 5,877,647, issued to Vajapey et al. and further in view of US Patent No. 4,386,286, issued to Kuo.

As per claim 6, this claim is a combination of claims 4 and 5, and therefore, it is rejected for the same reasons and motivations discussed in claims 4 and 5.

As per claim 17, rejected for the same reasons noted in claim 6.

Response to Arguments

7. Applicant's argument filed on 2/24/03 has been carefully considered but it is not found persuasive.

The argument is that the amended claim requires the first and second switchably conductive devices having control inputs commonly driven by a single driving signal (response paper number 18, page 13, lines 17-20) and Davis reference does not have this limitation.

As discussed in the preceding rejection, consider the "blackbox" comprises P4 and N2-N3, this "blackbox" having a control input terminal connected to the gate of N1 for receiving the same driving signal. Since the "blackbox" receives the driving signal at this terminal, this terminal is seen as a control input terminal, and since the "blackbox" allows current flow from VOUT to GND through the "blackbox" when the driving signal is increased to a certain voltage, it is proper to interpret the "blackbox" as a switchable conductive device.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink, appearing to read 'Minh Nguyen', with a horizontal line underneath.

10/17/03

Minh Nguyen
Primary Examiner
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